

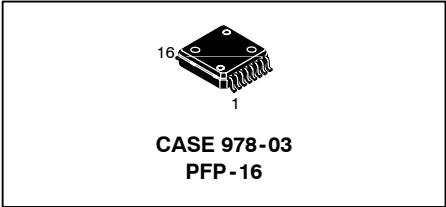
Replaced by MHVIC910HNR2. There are no form, fit or function changes with this part replacement. N suffix indicates RoHS compliant part.

MHVIC910HR2

**921 MHz - 960 MHz SiFET
 RF Integrated Power Amplifier**

**960 MHz, 10 W, 26 V
 GSM CELLULAR
 RF LDMOS INTEGRATED CIRCUIT**

The MHVIC910HR2 integrated circuit is designed for GSM base stations, uses Freescale's newest High Voltage (26 Volts) LDMOS IC technology, and contains a three-stage amplifier. Target applications include macrocell (driver function) and microcell base stations (final stage). The device is in a PFP-16 Power Flat Pack package which gives excellent thermal performances through a solderable backside contact.



- Typical GSM Performance @ Full Frequency Band (921 - 960 MHz), 26 Volts
 Output Power — 40 dBm (CW) @ P1dB
 Power Gain — 39 dB @ P1dB
 Efficiency — 48% @ P1dB
- On-Chip Matching (50 Ohm Input, DC Blocked, >5 Ohm Output)
- Integrated ESD Protection
- Usable Frequency Range — 921 to 960 MHz
- In Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain Supply Voltage	V_{DD}	28	Vdc
Gate Supply Voltage	V_{GS}	6	Vdc
RF Input Power	P_{in}	5	dBm
Case Operating Temperature	T_C	- 30 to + 85	°C
Storage Temperature Range	T_{stg}	- 65 to + 150	°C
Operating Channel Temperature	T_{ch}	150	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.9	°C/W

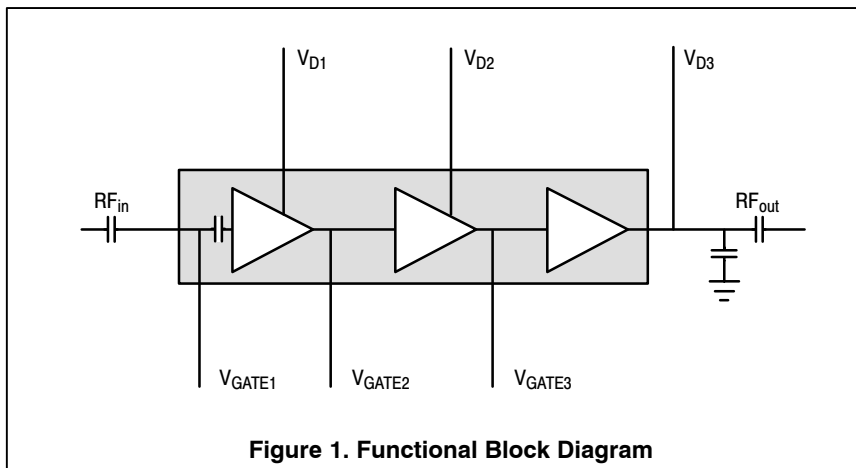


Figure 1. Functional Block Diagram

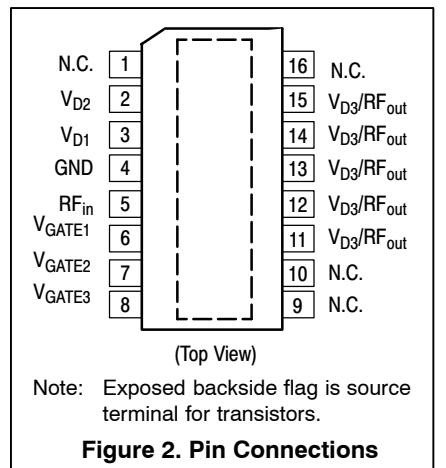


Figure 2. Pin Connections

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Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	0 (Minimum)
Machine Model	M2 (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	240	°C

Table 5. Recommended Operating Ranges

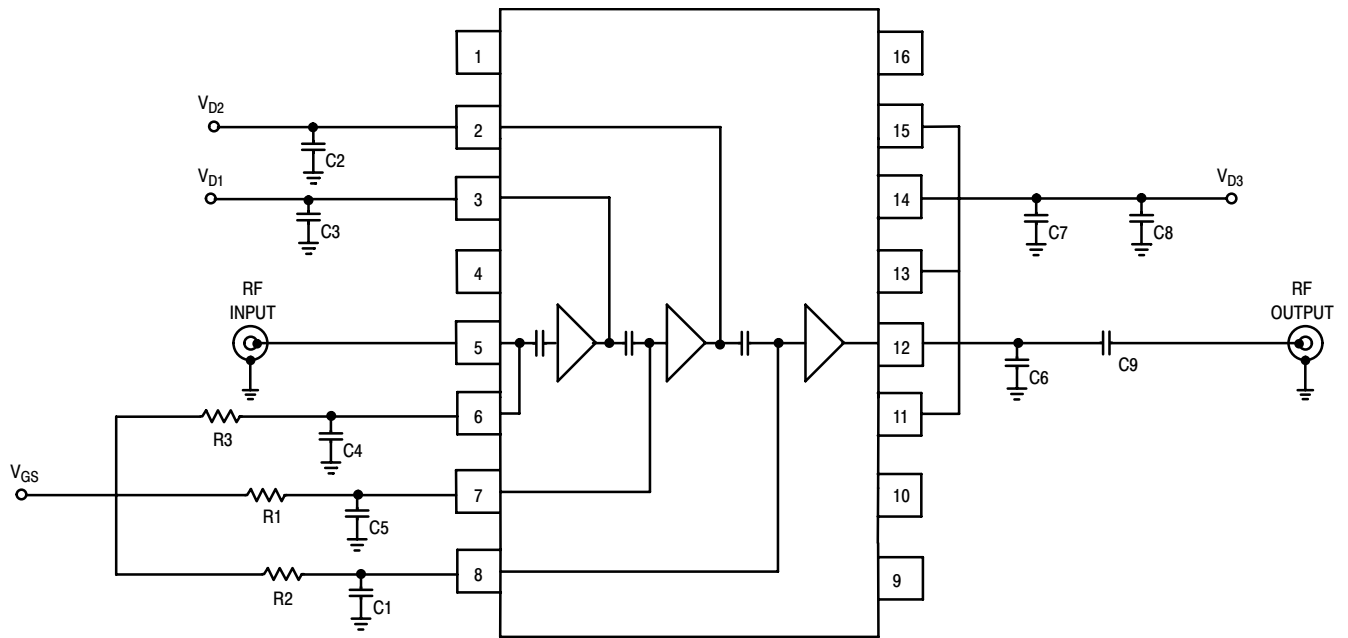
Parameter	Symbol	Value	Unit
Drain Supply Voltage	V_{DD}	26	Vdc
3rd Stage Quiescent Current	I_{DQ3}	150	mA
2nd Stage Quiescent Current	I_{DQ2}	50	mA
1st Stage Quiescent Current	I_{DQ1}	25	mA

Table 6. Electrical Characteristics ($T_A = 25^\circ\text{C}$ matched to a 50 Ω system, unless otherwise noted)

$V_{DD} = 26\text{ V}$, V_{GS} set for $I_{DQ3} = 150\text{ mA}$, frequency range 921-960 MHz

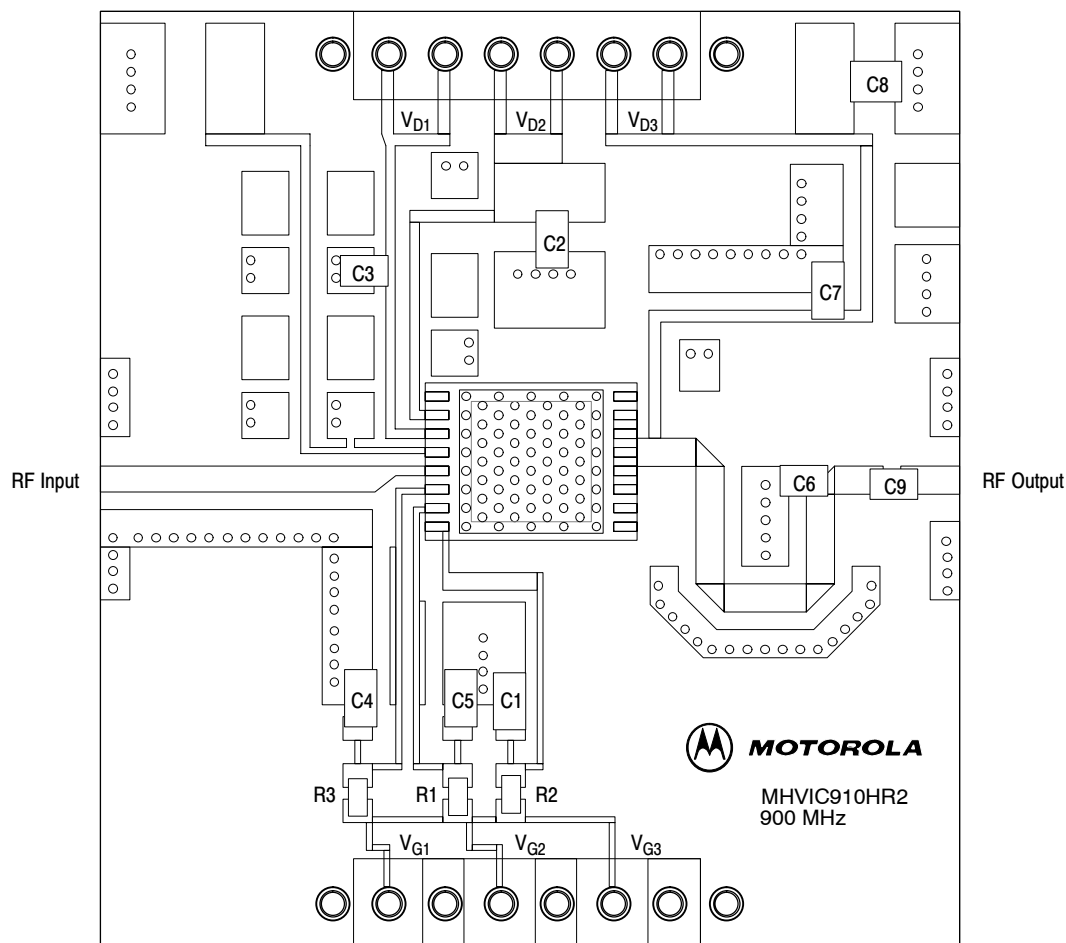
Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	f_{RF}	921	—	960	MHz
Output Power @ 1 dB Compression Point	P @ 1dB	39	40	—	dBm
Power Gain @ P1dB	G @ 1dB	38	39	—	dB
Power Added Efficiency @ 1 dB Compression Point	PAE @ 1dB	43	48	—	%
Input Return Loss @ P1dB	IRL @ 1dB	—	-15	-10	dB
Gain Flatness @ 40 dBm Variation ($T_C = -30$ to $+85^\circ\text{C}$ @ 40 dBm)	G_F G_V	— —	.5 5	— —	dB dB
Load Stability ($V_{DS} = 24\text{ V}$ to 28 V , $P_{out} = \text{P1dB Down to } 0\text{ dBm}$, All Phase Angles)	VSWR	10:1	—	—	—
Ruggedness ($V_{DS} = 26\text{ V}$, $P_{out} = 42\text{ dBm}$, Load VSWR = 10:1, All Phase Angles)	Ψ	No Damage After Test			

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.



- | | | | |
|------------------------|--|------------|---------------------------------------|
| C1, C2, C3, C4, C5, C8 | 1 μ F Surface Mount Chip Capacitors | J1, J2 | Header (Break-away), HDR2X10STIMCSAFU |
| C6 | 4.7 pF AVX Chip Capacitor, ACCU-P (08051J4R7BBT) | J3, J4 | SMA Connector 2052-1618-02 (Threaded) |
| C7 | 47 pF AVX Chip Capacitor, ACCU-P (08055K470JBTTTR) | R1, R2, R3 | 100 Ω Chip Resistors (0402) |
| C9 | 33 pF AVX Chip Capacitor, ACCU-P (08053J330JBT) | PCB | Rogers 04350, 20 mils |

Figure 3. 921-960 MHz Demo Board Schematic



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 4. 921 -960 MHz Demo Board Component Layout

TYPICAL CHARACTERISTICS

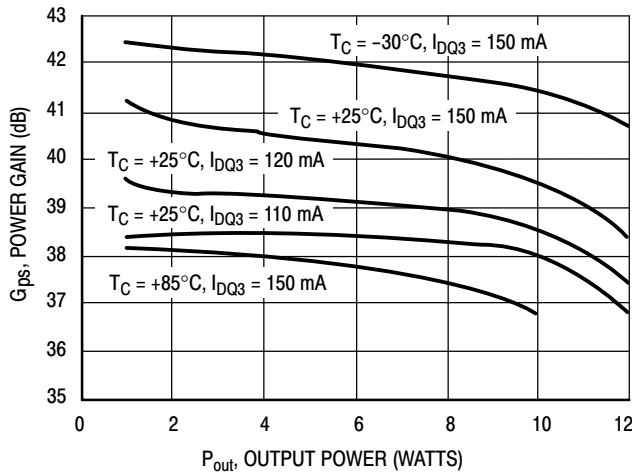


Figure 5. Power Gain versus Output Power

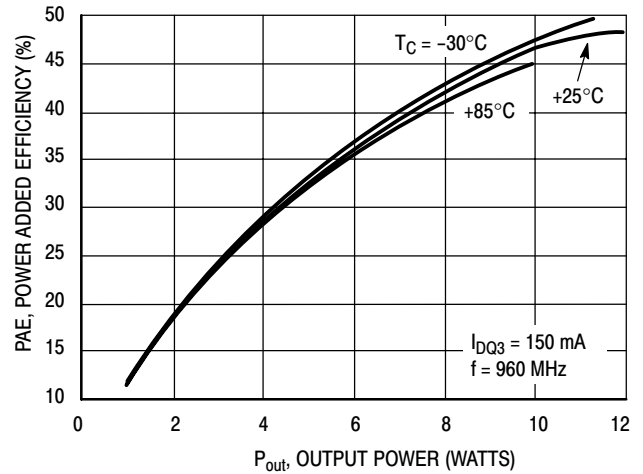


Figure 6. Power Added Efficiency versus Output Power

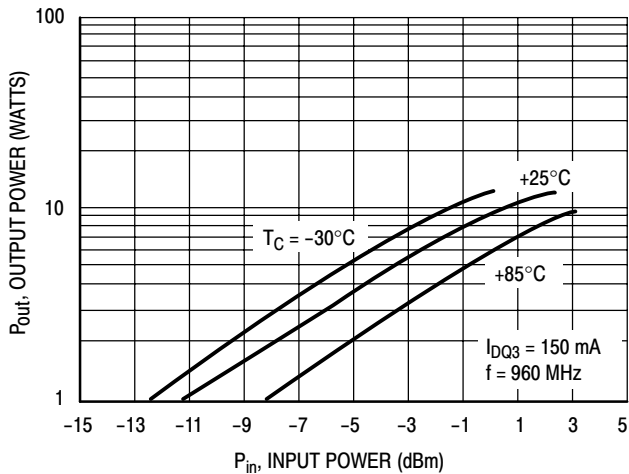


Figure 7. Output Power versus Input Power

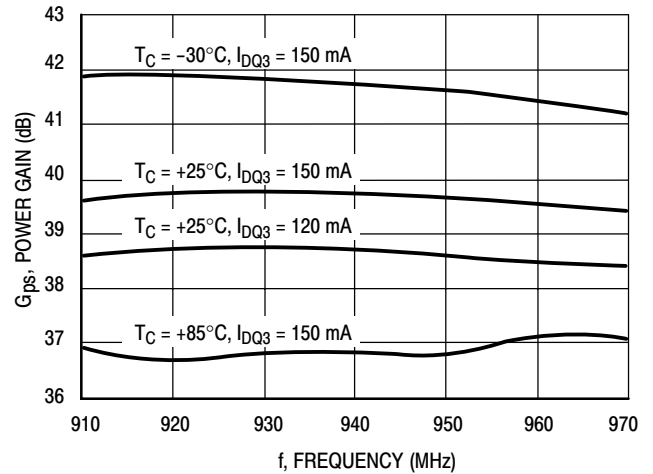


Figure 8. Power Gain versus Frequency
 $P_{out} = 10\text{ W}$

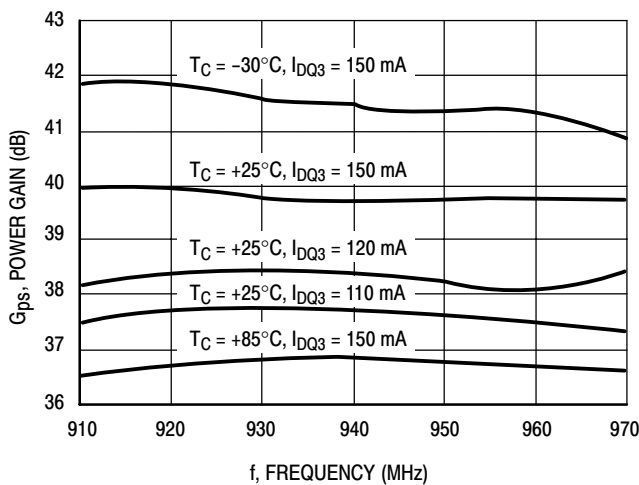


Figure 9. Power Gain versus Frequency
 $P_{out} = P_{1dB}$

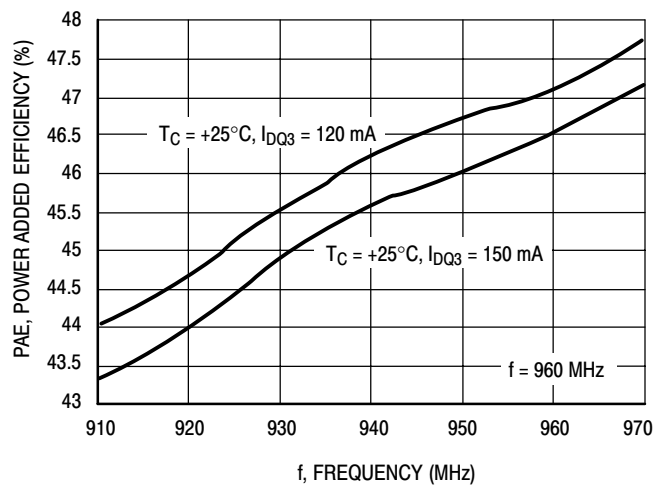


Figure 10. Power Added Efficiency versus Frequency
 $P_{out} = 10\text{ W}$

TYPICAL CHARACTERISTICS

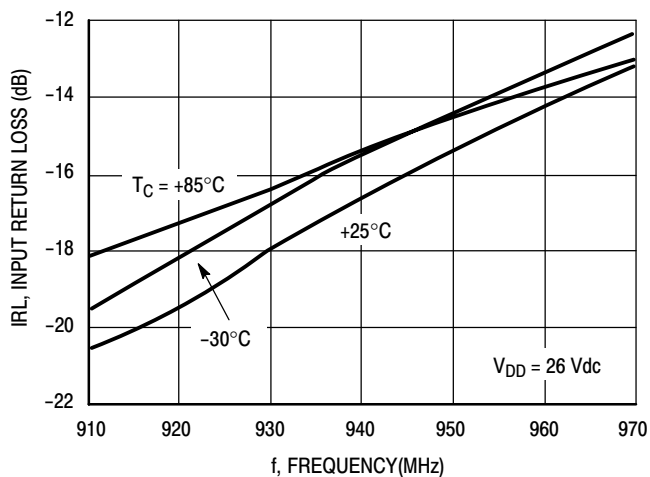


Figure 11. Input Return Loss versus Frequency
 $P_{out} = 10\text{ W}$

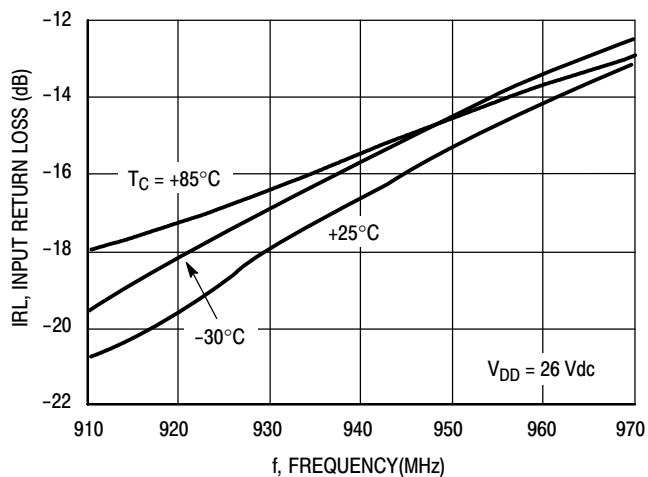


Figure 12. Input Return Loss versus Frequency
 $P_{out} = P_{1dB}$

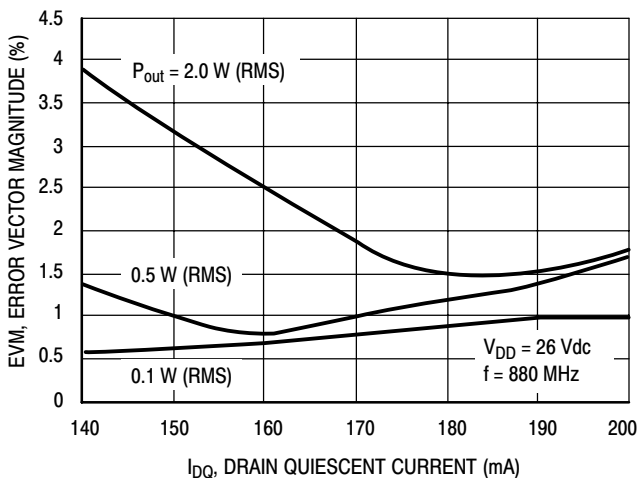


Figure 13. Error Vector Magnitude versus I_{DQ} Total

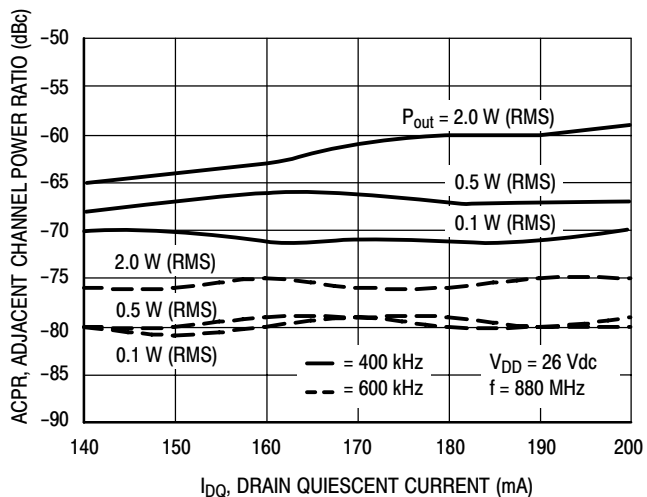


Figure 14. Adjacent Channel Power Ratio versus I_{DQ} Total

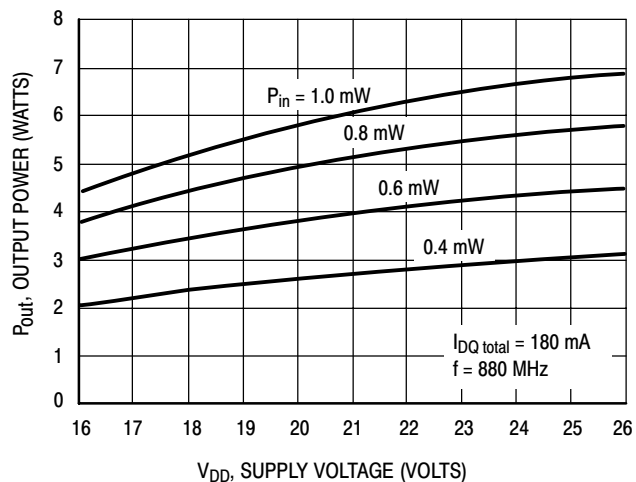


Figure 15. Output Power versus Supply Voltage

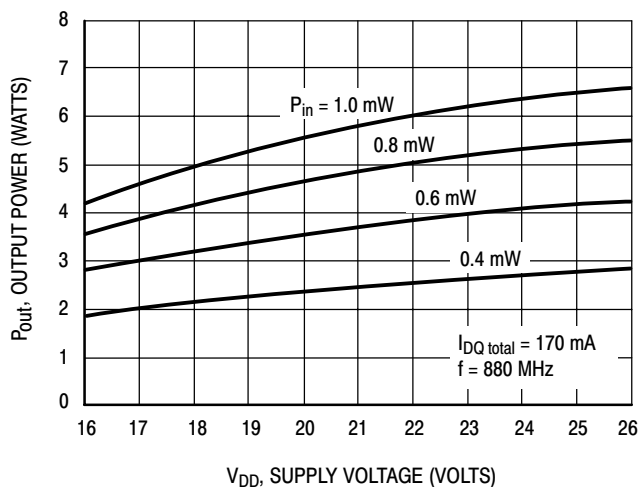


Figure 16. Output Power versus Supply Voltage

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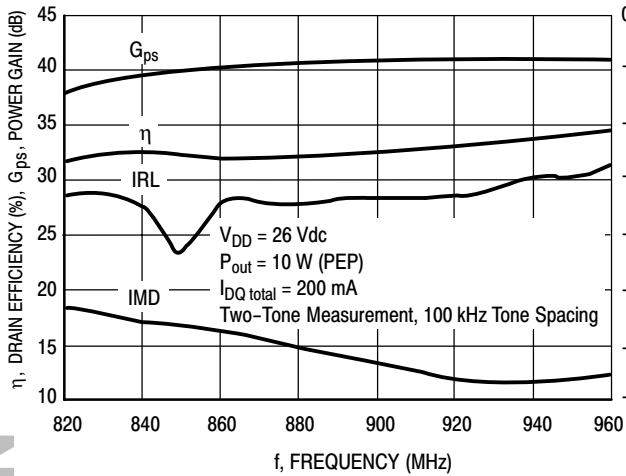


Figure 17. Two-Tone Broadband Performance

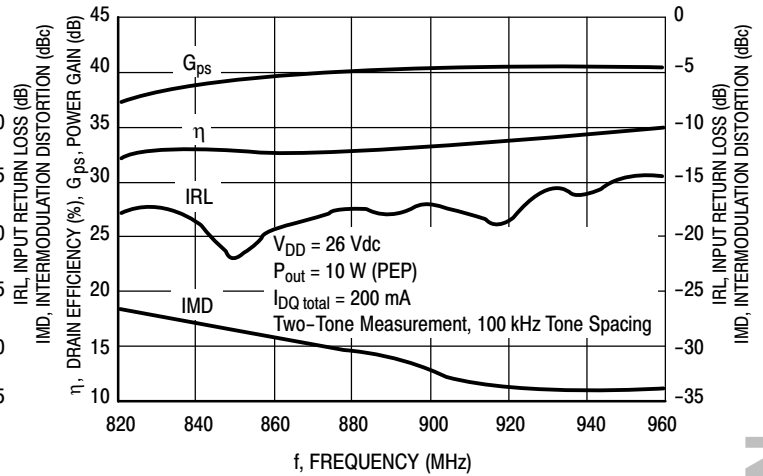


Figure 18. Two-Tone Broadband Performance

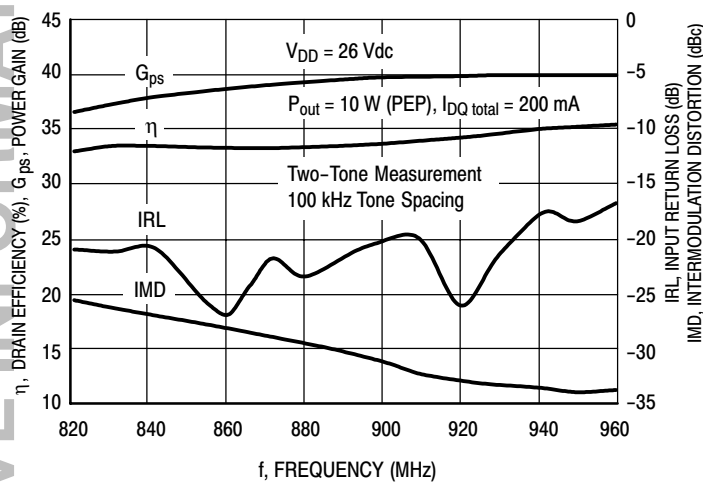


Figure 19. Two-Tone Broadband Performance

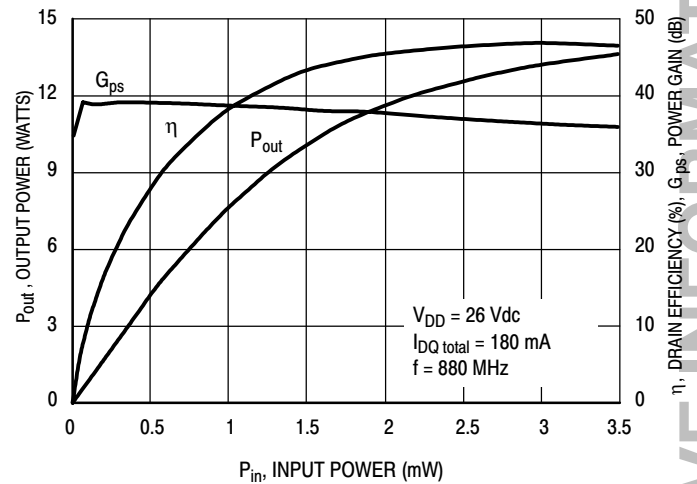


Figure 20. CW Performance @ 880 MHz

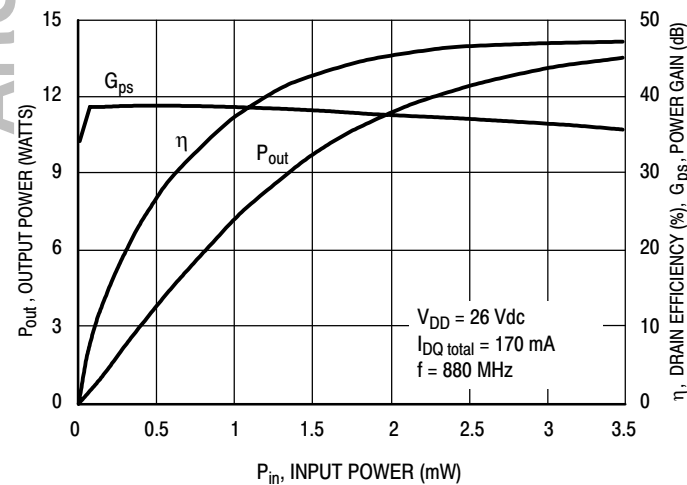


Figure 21. CW Performance @ 880 MHz

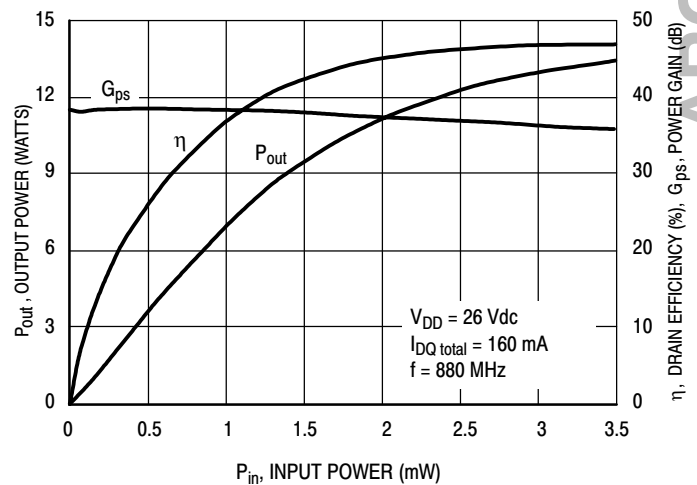


Figure 22. CW Performance @ 880 MHz

TYPICAL CHARACTERISTICS

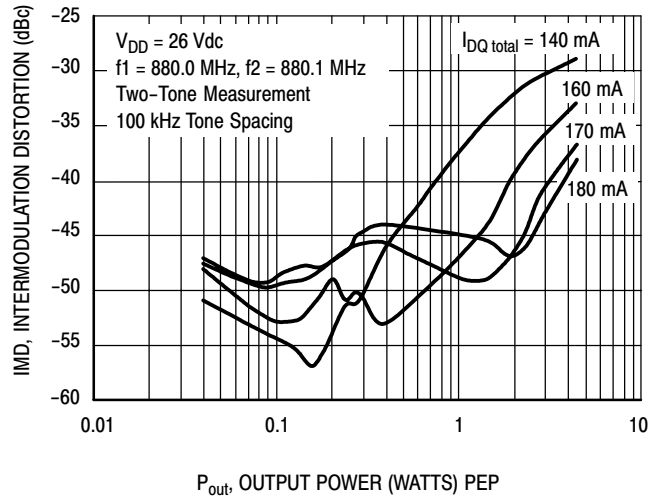


Figure 23. Intermodulation Distortion versus Output Power

$V_{DD} = 26\text{ V}$, $I_{DQ} = 225\text{ mA}$, $P_{out} = 40\text{ dBm}$

f MHz	Z_{load} Ω
900	$7.81 + j4.61$
920	$7.27 + j4.90$
940	$6.77 + j5.23$
960	$6.31 + j5.59$
980	$5.90 + j5.96$
1000	$5.53 + j6.36$

Z_{load} = Test circuit impedance as measured from drain to ground.

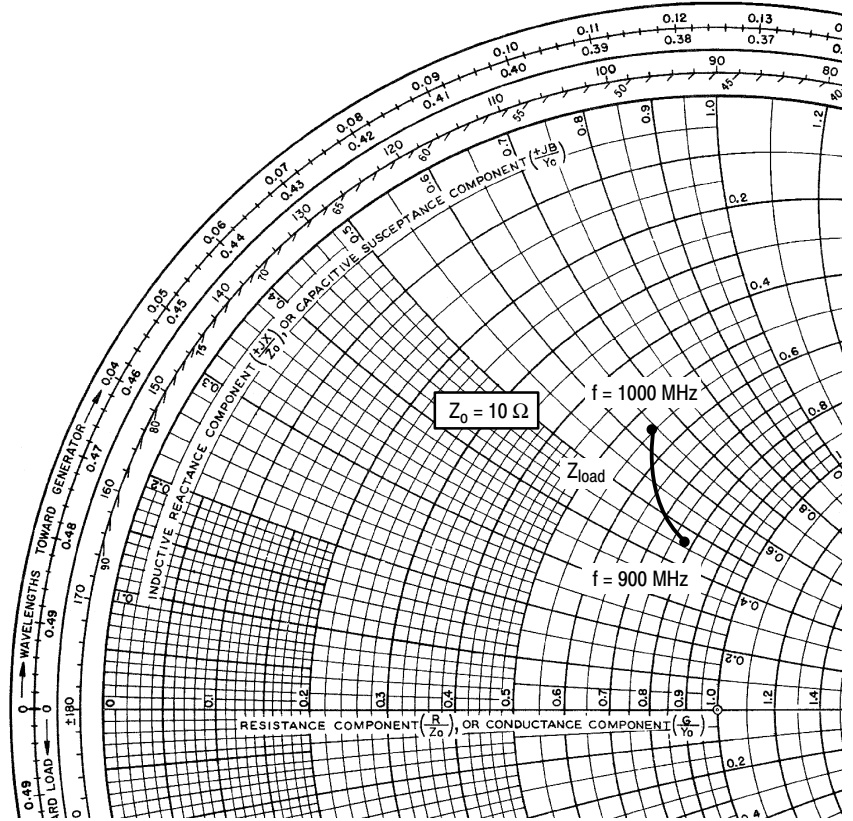
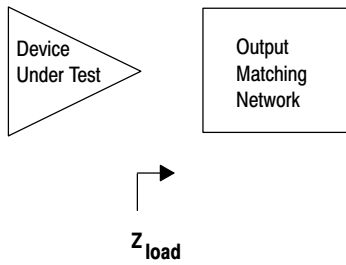
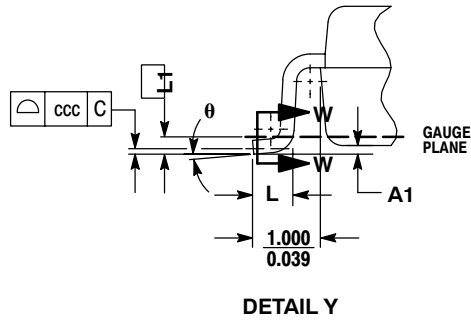
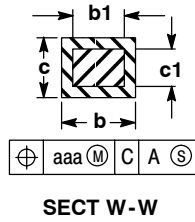
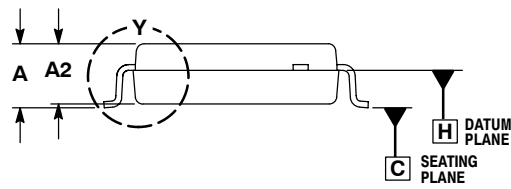
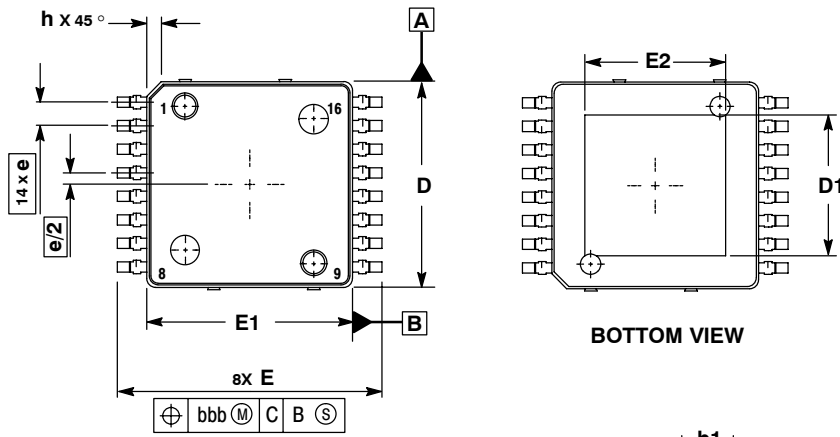


Figure 24. Series Equivalent Load Impedance

PACKAGE DIMENSIONS



NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

DIM	MILLIMETERS	
	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

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ISSUE C
PFP-16**

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